AMENDMENTS TO THE SPECIFICATION

Please amend the title as follows:

METHOD FOR MANUFACTURING CODE ADDRESS MEMORY CELL BY WHICH A STACK INSULATING FILM OF AN OXIDE FILM AND A NITRIDE FILM USED AS A DIELECTRIC FILM IN A FLASH MEMORY IS USED AS A GATE OXIDE FILM

After the paragraph ending page 6, line 11, please insert:

Figs. 5A-5D are views depicting the peripheral region being located separately from the cell region.

Please amend the paragraph spanning page 7, line 20-page 8, line 22, as follows:

A device isolation film is formed on a given region of the semiconductor substrate to define an active region and a device isolation region. The active region is defined into a cell region and a peripheral circuit region by a given process. Then, a tunnel oxide film 503 and a first polysilicon film 505 are formed on the ~~entire structure~~ semiconductor substrate 501 including the cell region and the peripheral circuit region as shown in Fig. 5A. Next, the first polysilicon film 505 and the tunnel oxide film 503 are patterned by means of lithography and etch process using a mask through a given region of the cell region is exposed. Due to this, a floating gate is defined in the cell region, and the tunnel oxide film 503 and the first polysilicon film 505 formed in the peripheral circuit region are completely removed as shown in Fig. 5B. After an insulating film 507 in which at least two or more layers of an oxide film and a nitride film are stacked is formed on the entire structure, a second polysilicon film 509 is formed as shown in Fig. 5C. [[A]] Referring to Fig. 5D, a pattering process from the second polysilicon film 509 to the tunnel oxide film 503 in the cell region is performed by means of lithography process and etch process using a mask through which a portion where the floating gate in the cell region is defined and a given portion of the peripheral circuit

region are exposed, thus forming a stack gate in which the floating gate and the control gate are stacked. At this time, the second polysilicon film 509 and the stack insulating film 507 in the peripheral circuit region are etched to form a gate. Thereafter, source and drain are formed in given regions of the cell region and the peripheral circuit region by means of impurity ion implantation process. Therefore, the flash memory cell is formed in the cell region and the CAM cell according to the present invention is formed in the peripheral circuit region. At this time, the stack insulating film 507 is used as the dielectric film between the floating gate 505 and the control gate 509 in the cell region and is also used as a gate oxide film between the semiconductor substrate 501 and the gate 509 in the peripheral circuit region.